TEXAS INSTRUMENTS

TPS60100, TPS60110 DC/DC Converter Evaluation Module

User's Guide

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Contents

Figures

Tables

Chapter 1

TPS60100 and TPS60110 EVM

The evaluation modules (EVM) for the new Texas Instruments (TI™) charge pump devices TPS60100 and TPS60110 help designers to evaluate the devices. The TPS60100 and TPS60110 charge pumps (also called switched capacitor DC/DC converters) are regulated voltage doublers.

With these EVMs it is possible to evaluate all different modes of the devices as well as their performance. Using jumpers to adjust the logic pin voltage levels, the devices can be set into the different modes. You only need a voltage source to test the operation of the devices.

The layout of charge pumps is critical, similar to the layout of inductive DC/DC converters. Therefore this given layout is a good tool to reduce evaluation-time for the designer.

Topic **Page**

1.1 Introduction

The Texas Instruments TPS60100 and TPS60110 charge pumps are regulated voltage doublers. The TPS60100 has an output voltage of 3.3 V from an input signal between 1.8 V and 3.6 V. The TPS60110 has an output voltage of 5 V from an input voltage between 2.7 V and 5.4 V. Both devices consist of two single-ended charge pumps that can operate either in phase (for minimum external components) or in anti-phase (for minimum output noise). For a description of the different operation modes and a functional description, please refer to the datasheets [literature number SLVS213A (TPS60100) and SLVS215 (TPS60110)].

The minimum number of external parts is three for the single-ended mode (both charge pumps operate in phase) or four in push-pull mode (the two charge pumps operate with 180° phase shift). The EVM is built up with six external parts for optimized performance.

The best performance of the charge pumps can be seen with ceramic capacitors. Actually this would be the most expensive solution because of the higher capacitive parts at the input and output. Therefore, on the TPS60100 or TPS60110 EVMs tantalum capacitors are used for the higher capacitive parts. To reduce the spikes during turnover from the transfer phase (charging of the output capacitor) of one charge pump to that of the other one, a ceramic capacitor is used in parallel with the tantalum ones at the input and output. Tantalum capacitors are not able to filter these spikes because their equivalent series resistance (ESR) is too high to act as fast as a ceramic one.

The flying capacitors have to be ceramic because they must be charged and discharged very fast and so their ESR has to be low. This criterion can only be reached with ceramic capacitors.

1.2 Schematic of the EVM

The schematics of the two EVMs for TPS60100 and TPS60110 are the same. The differences between the boards are the IC itself, the values for the external components (see Table 1–1), and the use of the connector 3V8. The connector 3V8 can be used on the EVM for TPS60100 to adjust the output voltage to 3.8 V. This mode is not implemented on the TPS60110. As long as you do not want to synchronize the TPS60110, connect this pin with a jumper to GND. When the TPS60100 or the TPS60110 is synchronized, the second pin of the connector 3V8 is used to apply the external clock signal.

Figure 1–1. Schematic of the Evaluation Module (EVM)

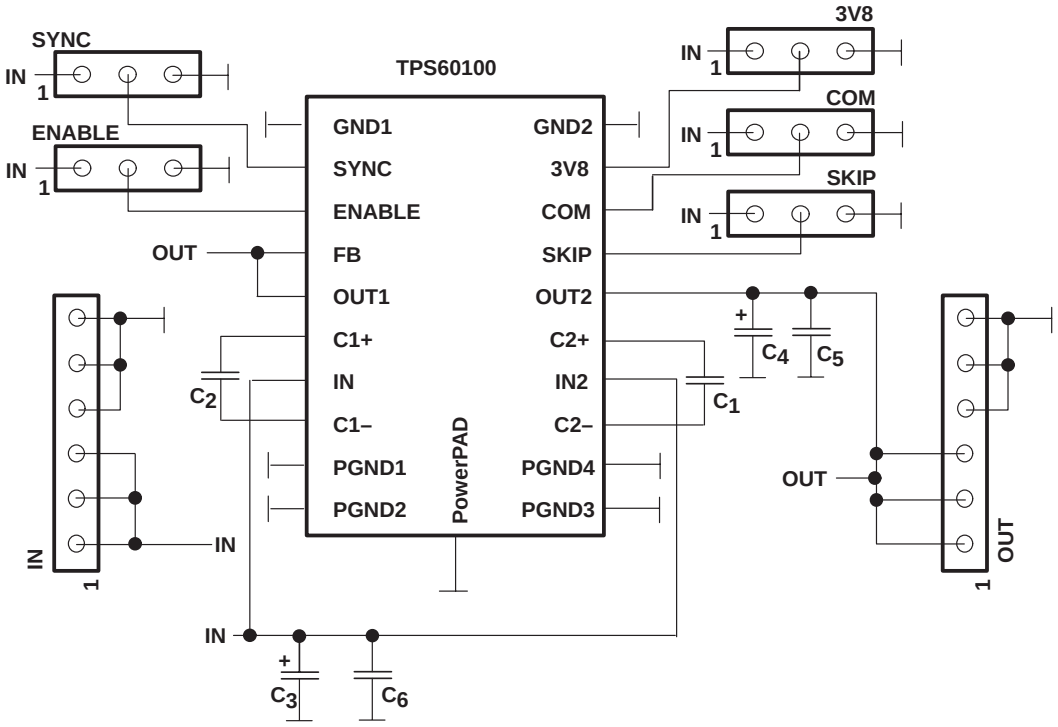

Table 1–1. Components on the EVM

COMPONENT	TPS60100	TPS60110	DESCRIPTION
C_1, C_2	2.2 µF, 16 V	2.2 µF, 16 V	Ceramic flying capacitors
C_3	10 µF, 16 V	15 µF, 16 V	Tantalum input capacitor
C_4	22 µF, 20 V	33 µF,16 V	Tantalum output capacitor
C_5, C_6	1 µF, 16 V	1 µF, 16 V	Ceramic help capacitors at input and output

Capacitors C_5 and C_6 are the two ceramic capacitors for reducing the spikes. If spikes are not critical in your application, it is possible to remove these two capacitors.

For the input and output of the voltage, there are two six-pin connectors on the board. Each has the first three pins for the supply (IN or OUT) and the last three pins for the ground (GND) signal.

The five three-pin connectors can be used to connect the five logic pins of the device. These pins are used to adjust the modes of the devices

(see Table 1–2). Each connector has the supply (In) signal at the first pin, the logic input at the second pin, and the ground (GND) signal at the third pin. So it is possible to use jumpers to connect the pin either to input (supply voltage) or to ground. It is also possible to connect any other signal by using an external signal source and connecting it to the second pin. These five pins are logic level CMOS inputs; for the specification of the levels, refer to the datasheets. The value of the signal connected to the logic pins can be higher than the supply voltage, but do not exceed the maximum ratings (see datasheets).

Leaving the second pin of these five three-pin connectors open is not allowed; either connect it via a jumper to the first or third pin, or use an appropriate external signal source with the appropriate signal level.

Table 1–2. Selected Modes by Connecting the Jumpers

Name	Connected to GND (Pin 3)	Connected to In (Pin 1)
3V8	3.3 V at the output (TPS60110: internal clock is used)	3.8 V at the output (TPS60110: Do not connect to IN)
Com	Push-pull mode	Single-ended mode
EN	Device is disabled	Device is enabled
Skip	Fixed-frequency mode	Pulse-skip mode
Sync	Device is internally synchronized	Device is externally synchronized, connect the external clock to the second pin of connector 3V8.

1.3 Layout of the EVM

Figure 1–2 and Figure 1–3 show the placement of the components and the layout of the EVM. Components are placed only on the top layer of the board. The signal on the bottom is the ground signal (GND). For good performance, the entire bottom layer is one GND plane, only interrupted by some vias.

Figure 1–2. Placement of the Components

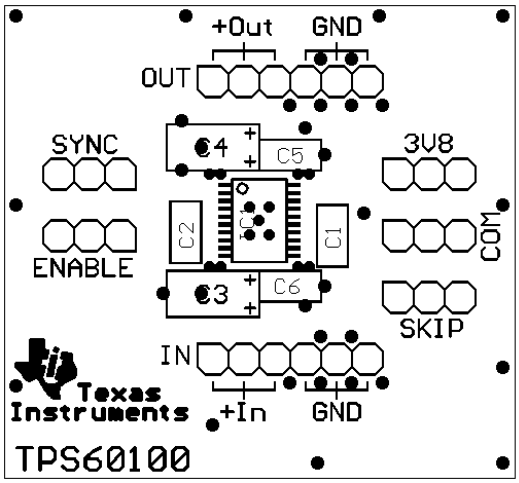

Figure 1–3. Top Layer of the EVM

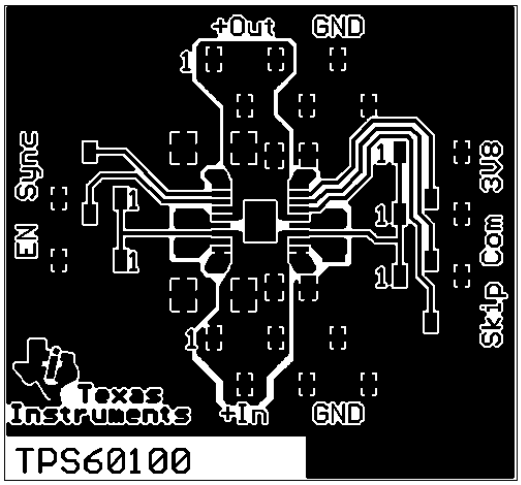

Table 1–1 contains the values and description of all 6 capacitors that are placed on the EVM.

The space needed for the IC and the capacitors on the EVM is around 15 mm × 16 mm = 240 mm^2. The capacitors are not optimized for space. They are optimized for performance. It is possible to use smaller capacitors to optimize the layout for minimum board space. On the EVM, it is also possible to solder some other capacitors because the pads are bigger than needed for the given capacitors.

1.4 Setup of the EVM

For proper operation of the EVM, follow these few steps:

1) Check if all five logic signals are properly connected, either jumper or external source.

2) Connect a load to the output (between GND and Out).
   TPS60100: 16.5 Ω to ∞Ω or 0 mA to 200 mA
   TPS60110: 16.7 Ω to ∞Ω or 0 mA to 300 mA

3) Connect a signal source (or a battery pack) with the appropriate voltage between the input (In) and ground, GND.
   TPS60100: 1.8 V to 3.6 V
   TPS60110: 2.7 V to 5.4 V